IN THE SPECIFICATION

Please amend the body of the "Brief Description of the Drawings," occurring on page 9, line 6 through page 10, line 11, as follows:

Figure 1 shows the flow through a generic logic synthesis system that features retiming, according to the prior art;

Figures 2a and 2b are schematic representations of an AND gate, according to the prior art;

Figure 3 is a schematic representation of a circuit in which a maximum achievable clock frequency is determined by the delay on the path A-F1, according to the prior art;

Figure 4 is a schematic representation of the circuit of Figure 3, in which a flip-flop F1 is retimed through a gate G, in effect creating two flip-flops F1a and F1b on the inputs of G, according to the prior art;

Figures 5a and 5b are schematic representations of circuits shown as examples of equivalent logic functions which present different retiming issues, according to the prior art;

Figure 6 is a schematic representation of a circuit to which a retiming algorithm can be applied, according to the prior art;

Figure 7 is a schematic representation of the circuit of Figure 6 as modified by adding negative delays and deleting registers in accordance with the invention;

Figure 8 is a schematic representation of an example circuit that illustrates how the steps of the invention modify a general procedure when cycles are present, according to the prior art;

Figure 9 is a schematic representation of the circuit of Figure 8 as modified by adding negative delays and deleting registers in accordance with the invention;

Figure 10 is a schematic representation of a circuit in which there is no way to break the cycle without breaking at least one forward path, according to the prior art; and

Figure 11 is a schematic representation of a circuit in which a forward path may be broken according to the invention.